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Hydrophone Preamplifier Optimization—Hybrid Microelectronics for Low-Noise Hydrophones

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This report presents a dc and low-frequency ac analysis of a low-noise preamplifier design. It also describes how the circuit has been miniaturized to hybrid form and packaged in a TO-99 can.

Since the early 1960's, remarkable growth has occurred in the quality of electronic amplifier design for underwater applications. The introduction of the junction field-effect transistor (JFET) resulted in hydrophone preamplifier designs having low-noise, high input impedance, broad bandwidth, and wide dynamic range. The further development of hybrid techniques has allowed these amplifiers to shrink greatly in size and cost. → next page

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20. ABSTRACT (Continued)

cont. The preamplifier circuit described has been optimized at the Underwater Sound Reference Detachment of NRL into a rugged integrated (hybrid) circuit suitable for low-noise hydrophone applications. Its self-noise is typically -118 dBV for a 1-GΩ input impedance. It operates on a single power supply and has a 100-kHz bandwidth. Equations are developed, suitable for programmable calculators, which analyze the ac and dc conditions in the circuit. An earlier report ("Hydrophone Preamplifier Optimization—Prediction of Hydrophone Self-Noise by a Noise Model," A. C. Tims, NRL Report 8180) gives a detailed analysis of the noise behavior of the circuit.

CONTENTS

HYDROPHONE PREAMPLIFIER OPTIMIZATION—
HYBRID MICROELECTRONICS FOR LOW-NOISE HYDROPHONES

INTRODUCTION

A prior report on "Hydrophone Preamplifier Optimization" [1] presented the prediction of hydrophone self-noise by a noise model. The acoustic sensor, coupling network, and preamplifier input stage were represented and analyzed by an equivalent-circuit noise model. This report presents the analysis and optimization of a low-noise preamplifier design and its miniaturization into a low-noise hybrid microelectronic circuit.

HISTORY

Since the early 1960's, with the advent of thin- and thick-film integrated circuits, changes have been phenomenal in all areas of electronics. Microelectronics ushered in a new era of electronic design philosophy; multitudes of components, functions, and capabilities could be realized using three to five orders of magnitude less physical space than prior circuitry. Integrated-logic circuits became the building blocks for digital systems, and the integrated operational amplifier (op-amp) became the building block for analog functions.

In the early 1960's the Naval Research Laboratory's Underwater Sound Reference Detachment (USRD) began to phase out the tube-type preamplifiers used in its standard hydrophones and began to use solid-state designs. This came about as a result of the proven reliability and effectiveness of the field-effect-transistor (FET) in high-impedance-input preamplifiers. By the late 1960's discrete-component solid-state designs had become the norm for standard hydrophone preamplifiers.

By the 1970's integrated circuit (IC) technology had advanced to the point that a variety of analog devices could be used in hydrophone preamplifiers. Many devices were used, but their roles have been relegated to such functions as second and succeeding amplifier stages, voltage regulators, and line drivers. In general, IC op-amps fail to perform satisfactorily with reactive inputs and have a very high self-noise compared to a discrete-FET input circuit. The latter disadvantage appears to be an innate failure of all IC op-amps.

The space-saving advantages of IC's for low-noise hydrophone applications can be realized by the use of custom-manufactured hybrid microelectronics. Performance of the hybrid, including self-noise, can be equal to or superior to its discrete-component counterpart.

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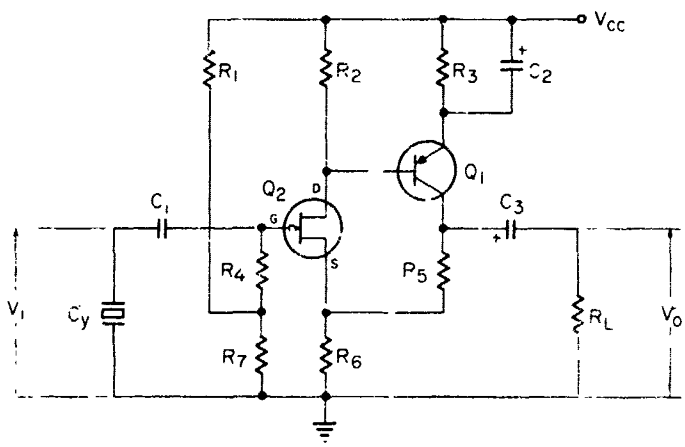


Fig. 1 — Preamplifier

PREAMPLIFIER DESCRIPTION

A schematic diagram of the preamplifier is shown in Fig. 1. The circuit can be tailored to interface with virtually any piezoelectric sensor. This preamplifier configuration has many features which make it especially suitable for hydrophone application. Some of these features are: single power-supply operation, low power dissipation, high input impedance, low output impedance, noninverting voltage gain, wide dynamic range, broad bandwidth, and low self-noise.

As Fig. 1 shows, the preamplifier circuit has two stages. The input stage is a low-noise junction field-effect transistor (JFET). The circuit is designed so that the gate-to-source and gate-to-drain junctions are reverse biased. This means that the JFET appears to be an open circuit when viewed from its gate terminal. The leakage current flowing out of the gate is usually negligible, especially at the low temperatures generally encountered by hydrophones.

Resistors R_1 and R_7 form a voltage divider, producing a gate bias V_G which is conducted to the gate terminal by R_4. Resistor R_4 is usually much larger than R_1 or R_7 and is essentially the input impedance of the preamplifier. The voltage produced by piezoelectric sensor C_y is coupled to the gate of Q_2 by capacitor C_1. The capacitance of C_1 is made much greater than that of C_y so that there is little signal loss through C_1.

The preamplifier output stage is formed by Q_1, R_3, C_2, and R_5. This is a common emitter stage whose output is fed back to the input stage by R_5. Negative direct-current (dc) feedback is achieved by R_3 and R_6, which stabilizes the dc biasing of the circuit.

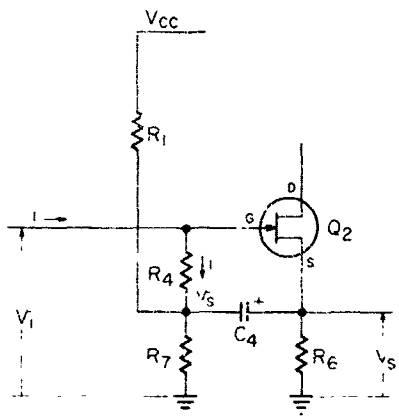
Bypass capacitor C_2 provides an alternating-current (ac) ground for the emitter of Q_1, increasing the gain of the output stage. The output signal is coupled to the load by C_3. The time constants R_3C_2 and R_LC_3 should be much larger than R_4C_y. If this is true, then the low-frequency rolloff of the circuit can be set by R_4 and C_y.

Because of the presence of C_2 the drain terminal of Q_2 will have little ac signal present. The feedback network formed by R_5 and R_6 forces the signal at the source and gate terminals of Q_2 to be nearly the same. This reduces the effects of the Q_2 junction capacitances, enhancing high-frequency operation. High-frequency rolloff can be introduced, if desired, by shunting R_5 with a small capacitor.

CIRCUIT VARIATIONS

Many variations of the circuit of Fig. 1 are possible, and some of the most common will be mentioned here.

Bootstrapping can be used to increase the effective input impedance. This is done by connecting a capacitor from the source terminal of Q_2 to the junction of R_1 and R_7, as shown in Fig. 2. For frequencies at which the impedance of C_4 is small compared to R_1 in parallel with R_7, the resistor R_4 is effectively multiplied by $1/(1 - v_s/v_i)$. The voltages v_s and v_i are nearly equal, leading to a large multiplication of R_4.



$$Z_1 = \frac{V_1}{I} \approx \frac{V_1}{\left(\frac{V_1 - V_S}{R_4}\right)} = R_4\left(\frac{1}{1 - \frac{V_S}{V_1}}\right)$$

PROVIDED $X_{C4} << (R_1 \,||\, R_7)$

Fig. 2 — Preamplifier with bootstrapping capacitor C_4

Diode protection can be added to the preamplifier at two points to greatly enhance its ruggedness, as shown in Fig. 3. Diode CR_1 protects the circuit against an inadvertent power-supply reversal. Diodes CR_2 and CR_3 protect Q_2 from voltage transients at the input and also prevent a buildup of dc potential across C_1. These diodes can be successfully implemented by using the collector-base junctions of low-noise transistors such as the 2N929. As long as v_i is less than about 0.8 V peak to peak, CR_2 and CR_3 do not conduct and usually have no effect on the circuit (the diodes do have a finite resistance which must be considered in the low-frequency rolloff). Larger values of v_i will be clipped, protecting Q_2. If

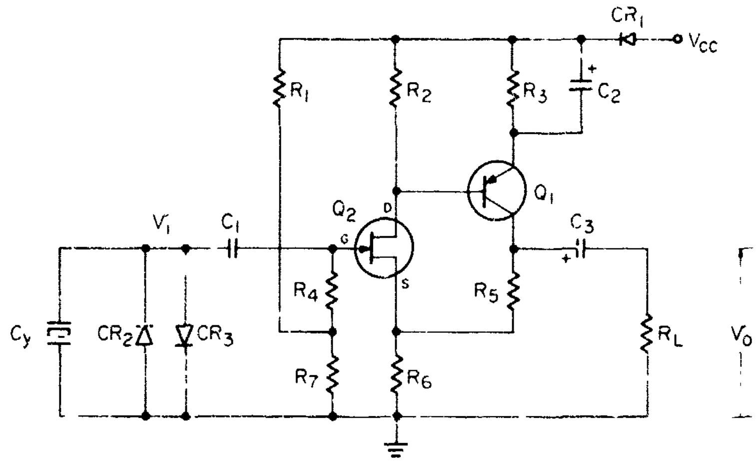


Fig. 3 — Preamplifier with protective diodes

more dynamic range is needed at the input, additional diodes can be placed in series with CR_2 and CR_3. This arrangement has not been found to increase the circuit noise.

When the preamplifier must drive a fairly long cable, a unity-gain buffer such as the LH0002 can be placed between C_3 and the collector of Q_1. Extremely long cables may require the addition of a voltage regulator between the circuit and the V_{CC} terminal.

CIRCUIT ANALYSIS, DC

Figure 4 shows the various dc voltages and currents in the preamplifier. If the circuit is properly biased, the gate of Q_2 is backbiased with respect to the source and drain. This means that

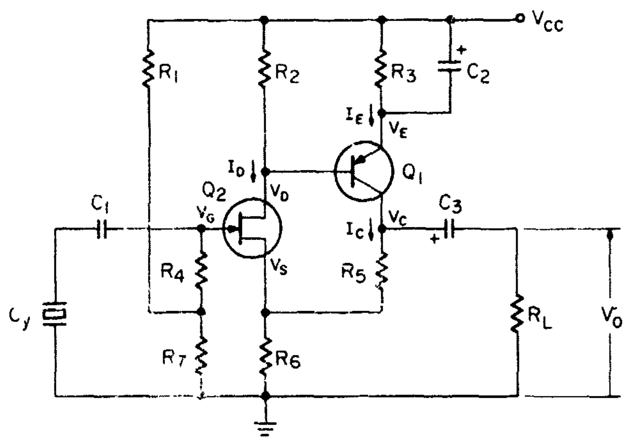
$$I_D < I_{DSS}. \tag{1}$$

(I_D, I_{DSS}, and other parameters are defined in Appendix A.) The JFET will be biased in the region of its characteristics, where the drain current is relatively independent of V_{DS}, or where

$$V_{DS} \geqslant V_{GS} - V_P. \tag{2}$$

If Eqs. (1) and (2) hold, then to a close approximation

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2. \tag{3}$$



(ALL VOLTAGES ARE WITH RESPECT TO GROUND)

Fig. 4 — Preamplifier with labels showing dc voltages and currents

To simplify this analysis, we may use with very small error

$$I_C \approx I_E. \tag{4}$$

The drain current is also defined by

$$I_D = \frac{I_E R_3 + V_{EB}}{R_2}\ , \tag{5}$$

if the base current of Q_1 is very small compared to I_D. Substituting Eq. (4) into Eq. (5) gives

$$I_D \approx \frac{I_C R_3 + V_{EB}}{R_2}\ . \tag{6}$$

Since I_D and I_C both flow in R_6,

$$V_S = (I_C + I_D) R_6. \tag{7}$$

Solving Eq. (6) for I_C yields

$$I_C = \frac{I_D R_2 - V_{EB}}{R_3}\ . \tag{8}$$

Substituting Eq. (8) into Eq. (7) gives

$$V_S = [I_D(R_2 + R_3) - V_{EB}]\ \frac{R_6}{R_3}\ . \tag{9}$$

If the gate leakage current of Q_2 can be neglected, then

$$V_G = \frac{V_{CC}R_7}{R_1 + R_7} . \tag{10}$$

Expanding Eq. (3) gives

$$\frac{I_D}{I_{DSS}} = \left(\frac{V_P - V_G + V_S}{V_P}\right)^2 . \tag{11}$$

Substituting Eq. (9) into Eq. (11) gives

$$\frac{I_D}{I_{DSS}} = \left[\frac{(V_P - V_G)R_3 - V_{EB}R_6 + I_D R_6(R_2 + R_3)}{R_3 V_P}\right]^2 . \tag{12}$$

Let

$$P = \frac{(V_P - V_G)R_3 - V_{EB}R_6}{R_3 V_P} \tag{13}$$

and

$$Q = \frac{R_6(R_2 + R_3)}{R_3 V_P} ; \tag{14}$$

then

$$\frac{I_D}{I_{DSS}} = (P + QI_D)^2, \tag{15}$$

which expands to

$$Q^2 I_D^2 + \left(2PQ - \frac{1}{I_{DSS}}\right) I_D + P^2 = 0. \tag{16}$$

This quadratic is solved in the usual way, yielding two solutions for I_D. One root however results in a solution for V_{GS} which is much less than V_P. This is clearly impossible, so that root is discarded. If we let

$$B = \frac{2P}{Q} - \frac{1}{Q^2 I_{DSS}} \tag{17}$$

and

$$C = \left(\frac{P}{Q}\right)^2, \tag{18}$$

then

$$I_D = \frac{-B - (B^2 - 4C)^{1/2}}{2} \tag{19}$$

Having obtained I_D and assuming a nominal V_{EB} of about 0.65 V dc, one obtains from Eq. (8) a solution for I_C. Equation (7) gives V_S. Then

$$V_C = V_S + I_C R_5, \tag{20}$$

$$V_E = V_{CC} - I_C R_3, \tag{21}$$

$$V_D = V_E - V_{EB}, \tag{22}$$

$$V_{DS} = V_D - V_S, \tag{23}$$

and

$$V_{GS} = V_G - V_S. \tag{24}$$

Having obtained this complete dc solution, one should then verify that Eqs. (1) and (2) do indeed hold and that

$$0 > V_{GS} > V_P. \tag{25}$$

As an example of this dc analysis, consider the circuit of Fig. 1 to be made up of the components in Table 1.

This circuit is designed for a power supply V_{CC} of +24 V dc. The 2N4867A JFET exhibits considerable variation in possible values of I_{DSS} and V_P. At room temperature

$$0.4 \leqslant I_{DSS} \leqslant 1.2 \text{ mA}$$

and (26)

$$-0.7 \geqslant V_P \geqslant -2 \text{ V dc}.$$

The JFET gate leakage current is typically 6 pA in this circuit at room temperature. The voltage drop which it produces across R_4 is therefore negligible. If the component values are assumed to be nominal, the dc analysis (Eqs. (3) through (24)) gives a room-temperature solution as shown in Table 2 with the JFET parameters varied over their full range.

Table 1 — Component Values for a Preamplifier Example

Component Designation	Value (or part)
Q_1	2N3251A
Q_2	2N4867A
R_1	500 kΩ
R_2	15 kΩ
R_3	13.3 kΩ
R_4	100 MΩ
R_5	23.7 kΩ
R_6	2.61 kΩ
R_7	30.1 kΩ
R_L	100 kΩ
C_1	0.01 μF
C_2	39 μF, 10 V
C_3	22 μF, 15 V
C_y	680 pF

Several things can be noted by examining Table 2. First, Eqs. (1), (2), and (25) are satisfied, so that the JFET is properly biased. Second, the collector voltage of Q_1 remains biased roughly midway between V_E and ground. The actual limits on the collector-voltage swing will be derived in the next section, but it can be seen that dc biasing influences the circuit's dynamic range. The data of Table 2 also allow one to select a proper voltage rating for the capacitors and to check quiescent power dissipation in each component.

The dc voltages measured in a preamplifier built from off-the-shelf components were as follows: V_C = 10.09 V dc, V_E = 19.33 V dc, V_S = 1.838 V dc, and V_G = 1.365 V dc.

CIRCUIT ANALYSIS, AC

This section will develop expressions for the low-frequency ac gain and output impedance. As mentioned earlier, the preamplifier input impedance is essentially R_4 at audio frequencies.

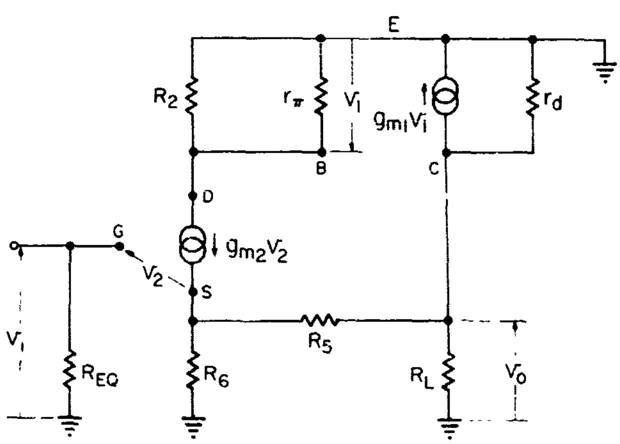
Figure 5 shows the low-frequency ac equivalent of the circuit in Fig. 1. (Appendix A defines the various parameters in the transistor models.) C_1, C_2, and C_3 are replaced by short circuits, and V_{CC} becomes an ac ground in the equivalent circuit of Fig. 5.

Low-Frequency Gain

To obtain the gain of this circuit, the configuration of Fig. 5 is progressively simplified as shown in Figs. 6a, 6b, and 6c. Using Fig. 6c, one can obtain v_s. This will allow v_o to be obtained using Fig. 6a.

Table 2 — DC Analysis of the Preamplifier Defined by Fig. 1 and Table 1

Parameter	Units	I_{DSS}, $\lvert V_P \rvert$				
		Minimum	Low	Nominal	High	Maximum
V_{CC}	V dc	24.00	24.00	24.00	24.00	24.00
I_{DSS}	mA	0.40	0.50	0.80	1.20	1.20
V_P	V dc	-0.70	-0.80	-1.10	-1.40	-2.00
V_C	V dc	8.05	8.47	9.67	10.99	12.21
V_E	V dc	20.31	20.11	19.56	18.94	18.38
I_D	mA	0.29	0.30	0.34	0.38	0.41
I_C	mA	0.28	0.29	0.33	0.38	0.42
V_G	V dc	1.36	1.36	1.36	1.36	1.36
V_S	V dc	1.47	1.54	1.75	1.98	2.19
V_D	V dc	19.71	19.51	18.96	18.34	17.78
V_{GS}	V dc	-0.11	-0.18	-0.39	-0.61	-0.82
V_{DS}	V dc	18.24	17.97	17.21	16.36	15.59



$$R_{EQ} = R_4 + \frac{R_1 R_7}{R_1 + R_7}$$

Fig. 5 — Low-frequency ac equivalent circuit

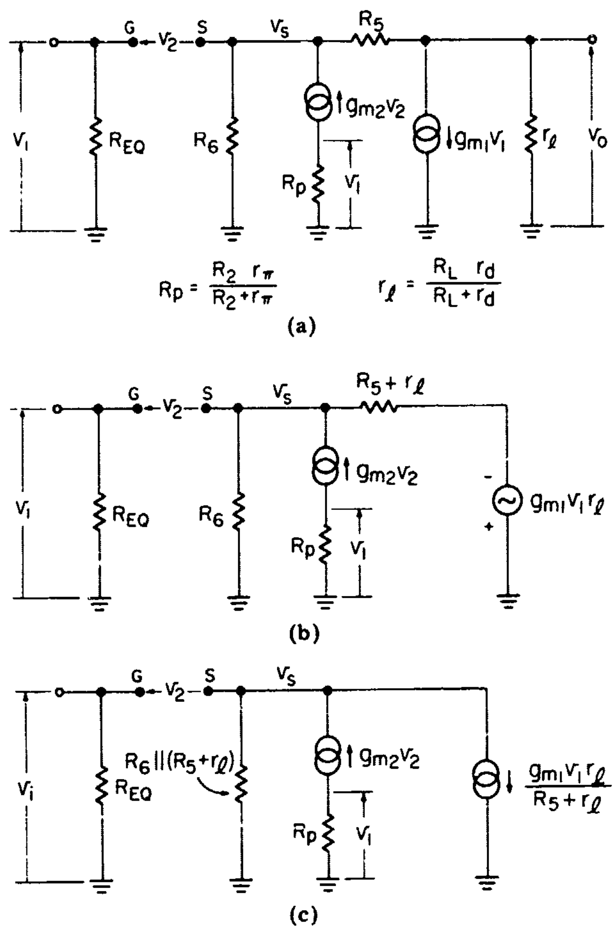


Fig. 6 — Progressive simplification of the circuit of Fig. 5

Referring to Fig. 6c and summing currents yields

$$g_{m_2} v_2 = \frac{g_{m_1} v_1 r_\ell}{R_5 + r_\ell} + \frac{v_s}{R_6 \| (R_5 + r_\ell)} . \tag{27}$$

Therefore

$$v_s = \left(g_{m_2} v_2 - \frac{g_{m_1} v_1 r_\ell}{R_5 + r_\ell} \right) \left[\frac{(R_5 + r_\ell) R_6}{R_5 + r_\ell + R_6} \right] . \tag{28}$$

But

$$v_1 = - g_{m_2} v_2 R_P . \tag{29}$$

Therefore

$$v_s = \left(g_{m_2} v_2 + \frac{g_{m_1} g_{m_2} v_2 R_P r_\ell}{R_5 + r_\ell} \right) \left[\frac{(R_5 + r_\ell) R_6}{R_5 + r_\ell + R_6} \right] . \tag{30}$$

Factoring and simplifying gives

$$v_s = g_{m_2} v_2 \left\{ \frac{R_6 [R_5 + r_\ell (1 + g_{m_1} R_P)]}{R_5 + r_\ell + R_6} \right\} . \tag{31}$$

Let

$$A = \frac{R_6 [R_5 + r_\ell (1 + g_{m_1} R_P)]}{R_5 + r_\ell + R_6} . \tag{32}$$

Then

$$v_s = A \, g_{m_2} v_2 . \tag{33}$$

As shown by Fig. 6a,

$$\frac{v_s - v_o}{R_5} = g_{m_1} v_1 + \frac{v_o}{r_\ell} , \tag{34}$$

from which

$$v_o = \frac{R_5 r_\ell}{R_5 + r_\ell} \left(\frac{v_s}{R_5} - g_{m_1} v_1 \right) . \tag{35}$$

Substituting Eq. (33) for v_s, Eq. (29) for v_1, and factoring gives

$$v_o = \left(\frac{r_\ell}{R_5 + r_\ell} \right) (g_{m_2} v_2)(A + g_{m_1} R_P R_5). \tag{36}$$

From Fig. 6

$$v_i = v_s + v_2 ; \tag{37}$$

therefore

$$v_i = v_2 (A \, g_{m_2} + 1). \tag{38}$$

Dividing Eq. (38) into Eq. (36) gives the gain:

$$G = \frac{v_o}{v_i} = \frac{g_{m_2} r_\ell (A + g_{m_1} R_P R_5)}{(R_5 + r_\ell)(A\, g_{m_2} + 1)} \quad . \tag{39}$$

If r_ℓ is allowed to become extremely large, then

$$G = \frac{v_o}{v_i} \approx \frac{g_{m_2}(A + g_{m_1} R_P R_5)}{A\, g_{m_2} + 1} \tag{40}$$

and

$$A \approx R_6(1 + g_{m_1} R_P). \tag{41}$$

Combining Eqs. (40) and (41) gives

$$G = \frac{v_o}{v_i} \approx \frac{R_6 + g_{m_1} R_P (R_5 + R_6)}{R_6(1 + g_{m_1} R_P) + (1/g_{m_2})}$$

$$\approx \frac{g_{m_1} R_P (R_5 + R_6)}{(1 + g_{m_1} R_P) R_6} \tag{42}$$

$$\approx \frac{R_5 + R_6}{R_6} \quad , \quad r_\ell \to \infty . \tag{43}$$

As an example, consider again the circuit of Fig. 1 and the component values of Table 1. The nominal operating points for Q_1 and Q_2 were already derived and presented in Table 2. For the 2N3251A transistor the manufacturer's data give a typical h_{fe} of 170 (at V_{CE} = 10 V, I_C = 0.33 mA, f = 1 kHz, and T_A = 25°C). Therefore

$$g_{m_1} \approx 38.9\, I_C = 12.84 \text{ mS},$$

$$r_\pi = h_{fe}/g_{m_1} = 13.24 \text{ k}\Omega,$$

and

$$R_P = r_\pi \,||\, R_2 = 7.03 \text{ k}\Omega.$$

Also from manufacturer's data, $r_d = 1/h_{oe} \approx 100$ kΩ. Let R_L = 100 kΩ. Then $r_\ell = R_L \,||\, r_d$ = 50 kΩ. For the 2N4867A JFET

$$g_{m_2} = \frac{-2\, I_{DSS}}{V_P}\left(1 - \frac{V_{GS}}{V_P}\right). \tag{44}$$

With use of the nominal values in Table 2, g_{m_2} = 0.939 mS. Solving Eqs. (32) and (39) gives $A = 156.9 \times 10^3$ and $G = v_o/v_i = 9.86 = 19.88$ dB for R_L = 100 kΩ. Now let R_L = open circuit. Then $r_\ell = r_d$ = 100 kΩ. Again solving Eqs. (32) and (39) gives $A = 189.1 \times 10^3$ and $G = v_o/v_i = 9.90 = 19.91$ dB for R_L = open circuit.

The actual measured gain in a constructed preamp was 19.7 dB for R_L = 100 kΩ and f = 1 kHz.

Maximum Output Voltage

If the input signal v_i is continuously increased, the output signal v_o will ultimately be distorted or clipped. To maximize the output dynamic range, one attempts to bias the circuit so that the collector voltage v_c clips equally at both ends, as in Fig. 7a.

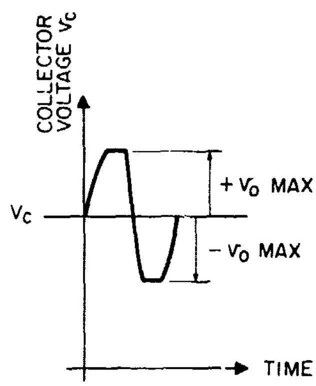


Fig. 7a — Clipping of the collector voltage

In the positive direction the collector voltage can rise until Q_1 is saturated and $v_c \approx V_E$. Therefore

$$+ v_o \text{ MAX} \approx V_E - V_C, \tag{45}$$

where + v_o MAX is the maximum positive swing of the output signal.

In the negative direction the collector voltage can fall until Q_1 is cut off and the collector current becomes zero. In this case $v_c \approx v_s$, where v_s is the signal on the source terminal of Q_2. This is illustrated in Fig. 7b. For this case,

$$V_C - (- v_o \text{ MAX}) \approx V_S - (- v_o \text{ MAX})\left(\frac{R_6}{R_5 + R_6}\right), \tag{46}$$

where - v_o MAX is the maximum negative swing of the output signal. Solving Eq. (46) gives

$$- v_o \text{ MAX} \approx (V_C - V_S)\left(\frac{R_5 + R_6}{R_5}\right). \tag{47}$$

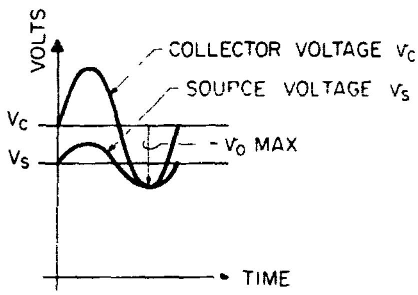


Fig. 7b – Distortion of the negative swing of v_c as it meets v_s

Equation (46) assumes that R_L is an open circuit and that $i_d << i_c$. For finite but large loads, clipping occurs somewhat sooner than predicted by Eq. (47).

Low-Frequency Output Impedance

The equivalent circuit of Fig. 5 is redrawn in Fig. 8. For this analysis, v_i is short circuited, and a signal source v_o is connected at the load terminals in place of R_L. As shown by Fig. 8b,

$$i_o = g_{m_1} v_1 + \frac{v_o}{r_d} + i_{R_5}. \tag{48}$$

But

$$v_1 = -g_{m_2} v_2 R_P. \tag{49}$$

Therefore

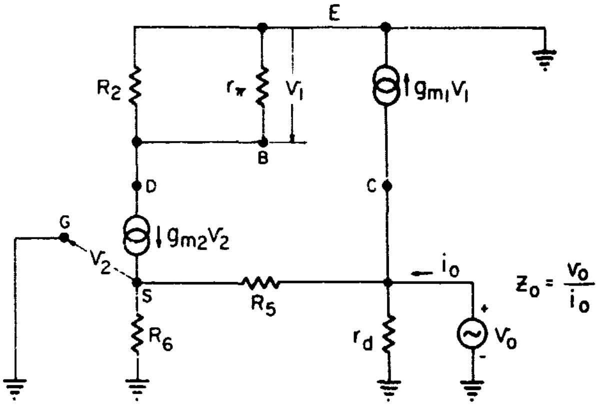
$$i_o = \frac{v_o}{r_d} + i_{R_5} - g_{m_1} g_{m_2} v_2 R_P; \tag{50}$$

also

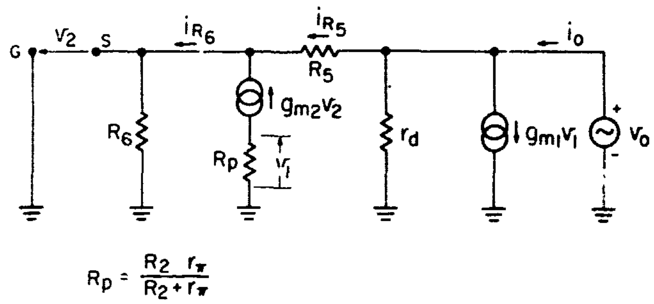
$$i_{R_5} = \frac{v_o + v_2}{R_5}. \tag{51}$$

Substituting Eq. (51) into Eq. (50) gives

$$i_o = v_o \left(\frac{r_d + R_5}{r_d R_5} \right) + v_2 \left(\frac{1 - g_{m_1} g_{m_2} R_P R_5}{R_5} \right). \tag{52}$$



(a) Patterned after Fig. 5



(b) Simplified equivalent circuit

Fig. 8 — Preamplifier low-frequency ac equivalent circuit arranged for deriving z_0

An expression is needed for v_2:

$$v_2 = -i_{R_6} R_6 = -(i_{R_5} + g_{m_2} v_2) R_6$$

$$= -\left(\frac{v_o}{R_5} + \frac{v_2}{R_5} + g_{m_2} v_2\right) R_6. \tag{53}$$

Solving Eq. (53) for v_2 gives

$$v_2 = -v_o \left[\frac{R_6}{R_5 + R_6(1 + g_{m_2} R_5)}\right]. \tag{54}$$

Substituting Eq. (54) into Eq. (52) and solving for $Z_o = v_o/i_o$ yields

$$Z_o = \frac{r_d[R_5 + R_6(1 + g_{m_2}R_5)]}{R_5 + R_6(1 + g_{m_2}R_5) + r_d[1 + g_{m_2}R_6(1 + g_{m_1}R_P)]} , \tag{55}$$

where $r_d = 1/h_{oe}$.

As an example, consider again the circuit of Fig. 1 with the component values of Table 1 operating at a frequency of 1 kHz. Values have already been obtained for the terms in Eq. (55). These are

$$g_{m_1} = 12.84 \text{ mS},$$

$$g_{m_2} = 0.939 \text{ mS},$$

$$R_P = 7.03 \text{ k}\Omega,$$

$$r_d = 100 \text{ k}\Omega,$$

$$R_5 = 23.7 \text{ k}\Omega,$$

and

$$R_6 = 2.61 \text{ k}\Omega.$$

Substituting these into Eq. (55) yields $Z_o = 374.2\ \Omega$, resistive.

(The important equations in this report are summarized in Appendix B.)

OPERATING CHARACTERISTICS

Table 3 summarizes the operating characteristics of the preamplifier configuration of Fig. 1.

CIRCUIT MINIATURIZATION

The circuit of Fig. 1 less capacitors lends itself to implementation as a hybrid IC. Eltec Instruments, Inc., Daytona Beach, Florida, under contract to USRD, has packaged this circuit in a low-profile TO-99 can. These have been produced in small quantities at a cost to the Navy of $40 each. A practical example of such a circuit is shown schematically in Fig. 9. Only the addition of C_1, C_2, and C_3 is required to have a complete preamplifier.

A broad line of highly stable, reliable, thin- and thick-film components and a variety of semiconductor chips are available for hybrid applications. The particular devices specified for this hybrid were used because of prior experience and noise data accumulated from earlier discrete component designs (Appendix C).

Table 3 — Operating Characteristics

Characteristics	Typical Value(s)
Power supply	+12 V dc to +36 V dc
Power dissipation	<30 mW
Input impedance	Up to 1 GΩ
Output impedance	≈500 Ω
Noninverting voltage gain	0 to +30 dB
Dynamic range	>100 dB
Bandwidth	100 kHz (low-frequency cutoff determined by sensor impedance)
Self-noise	-118 dB V broadband for 1 GΩ input impedance
Input capacitance	12 to 14 pF

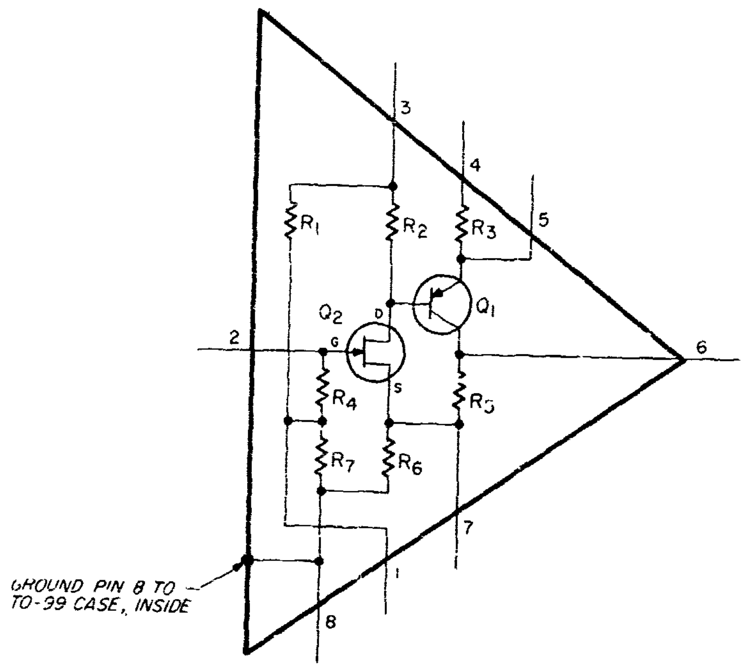


Fig. 9 — Hybrid integrated circuit

Q_2 is an N-channel, depletion-mode, silicon JFET (Siliconix type CHP, geometry NS, Siliconix Inc., Santa Clara, Calif.). The NS chip is used for the 2N4867-69 series of transistors. These are ultralow-noise FET's specifically designed for infrasonic and audio frequency applications.

A general-purpose small-signal bipolar transistor is used for Q_1. It is obtained from Semiconductor Services, Inc., Salem, Mass., and identified as semiconductor chip process 69, PNP, small signal. This chip is used for the 2N3251A transistor.

Tantalum nitride film resistors are used for R_1 through R_7 excluding R_4. Tantalum nitride film resistors have a noise index comparable to high-quality discrete metal-film resistors. Series SFM, Format A, from National Micronetics, Inc., Semi-Film Division, West Hurley, N.Y., are specified. The manufacturer claims a maximum noise index of -30 dB or 0.032 μV/V per decade for the resistors. All resistance values are as given in Table 1 with a $\pm 1\%$ tolerance.

The high-megohm chip resistor used for R_4 is a film-resistive glass with thick-film gold terminals. It is an Eltec Model 114 high-megohm chip from Eltec Instruments, Inc.

Each component chip is bonded with epoxy adhesive to the header of a TO-99 case. The circuit is then connected using 0.001 gold wire. The wire is ultrasonically ball-bonded to bond pads on the chips. Figure 10 is a photograph of the completed circuit enlarged about 10 times. A unit is completed by hermetically sealing the circuit in a low-profile can.

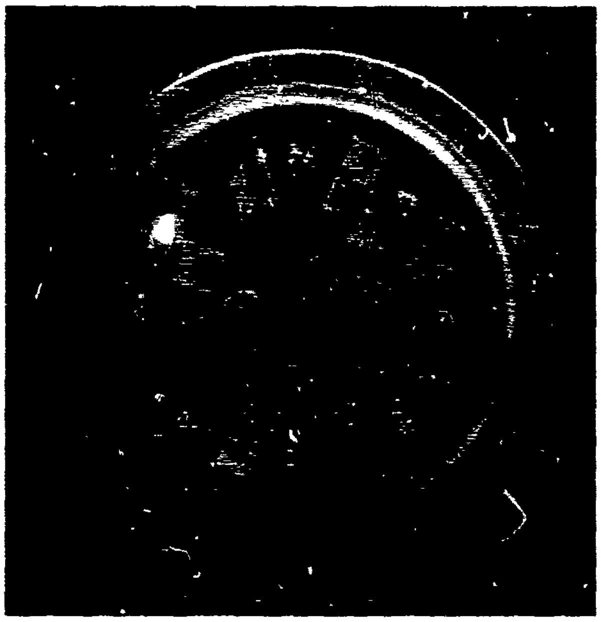


Fig. 10 — Hybrid circuit magnified 10X (photograph from Eltec Instrs, Inc.)

The choice of pins on the package, although somewhat arbitrary, allows trimming certain components externally. The pins chosen in this design allow good communication with

the internal circuit and provide flexibility in experimental hydrophone designs. The pins are also convenient test points for production and incoming inspection.

ADVANTAGES OF HYBRIDS

There are several advantages to this hybrid approach. The most important is that the preamplifier is much smaller than its discrete version. The size of the hydrophone preamplifier case can be reduced and in some instances eliminated all together. The preamplifier can be included inside a cylindrical sensor element, or it may be constructed on an aluminum oxide end cap of a capped-cylinder hydrophone.

The cost of constructing and repairing a practical preamplifier is also reduced, since there are so few components. Inventories of hybrid circuits are easier to acquire and maintain than the equivalent assortment of printed-circuit boards and discrete components.

The performance of the hybrid circuit has equaled or exceeded that of the discrete version. Self-noise levels are more consistent, because the components are sealed and electrically shielded within the TO-99 housing. Also, critical high-impedance circuit points about the gate of the FET are more environmentally stable.

SELF-NOISE

For self-noise measurements, the hybrid was used in the circuit configuration shown in Fig. 1 with the component values as given in Table 1, except that the value of C_1 was increased to 1 μF. The self-noise was measured using a Federal-Scientific Model UA-14 Spectrum Analyzer (400-resolution-line real-time spectrum analyzer) and a Federal-Scientific Model 1014 Spectrum Averager (which digitally sums and averages successive spectra).

Figure 11 shows the self-noise of the hybrid with various values of sensor capacitances. The noise voltage measured at the output of the preamplifier (E_{no}) is indicated at the right side of the figure, and the equivalent input noise voltage (E_{ni}) is indicated at the left side. E_{ni} is given by

$$E_{ni}\ (\mathrm{dB}) = E_{no} - G,$$

where G is the preamplifier voltage gain (20 dB).

If an open-circuit crystal sensitivity of -183 dB re 1 V/μPa is assumed for a particular hydrophone using the hybrid circuit, then the end-of-cable hydrophone sensitivity (M_e) would be -163 dB re 1 V/μPa. The equivalent noise pressure (P_{en}) is

$$P_{en}\ (\mathrm{dB}) = E_{no} - M_e.$$

The equivalent noise pressure for a sensor with capacitances of 100 pF, 1000 pF, and 1 μF and with the assumed M_e is shown in Fig. 12. Knudsen's sea-state-zero is indicated as a reference in this figure.

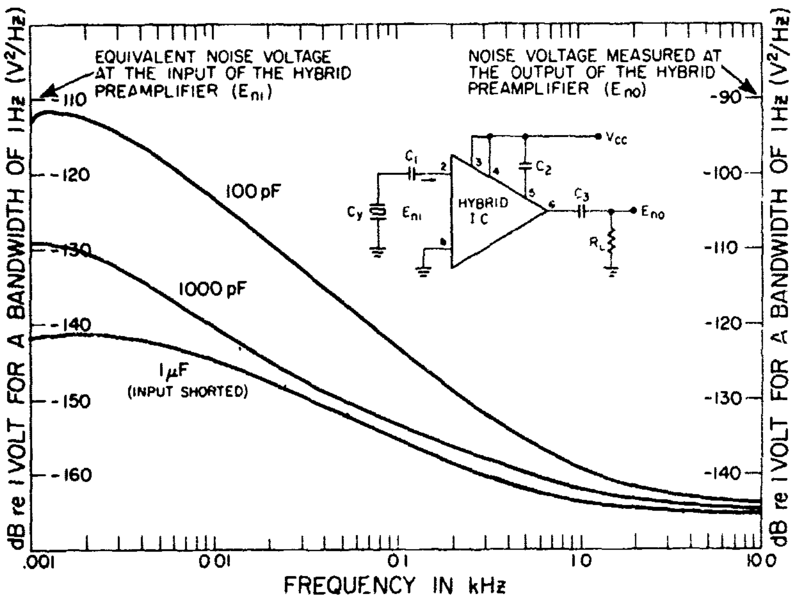


Fig. 11 — Self-noise of the hybrid circuit with various sensor capacitances

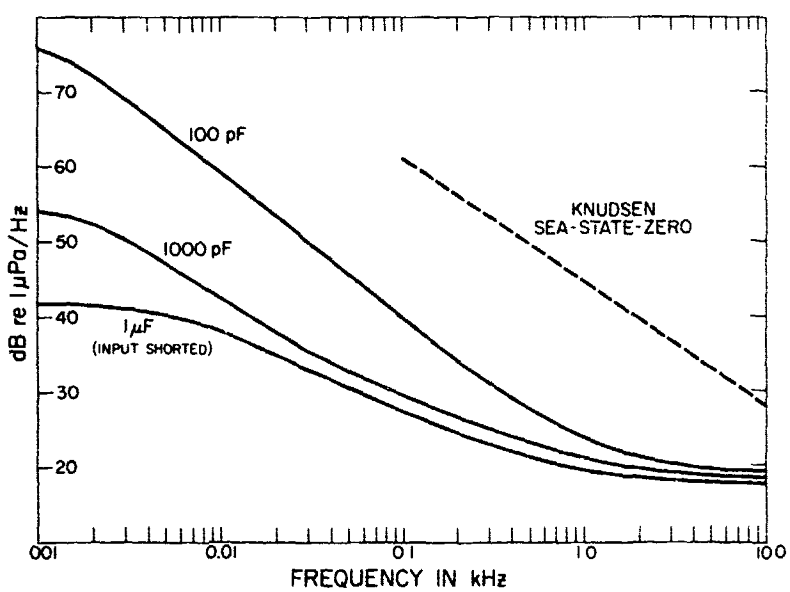


Fig. 12 — Equivalent noise pressure for a hydrophone with various sensor capacitances

The broadband equivalent input noise of the hybrid, measured using a B&K random-noise voltmeter in the frequency range 2 Hz to 20 kHz, is 8 μV (-102 dBV) for a 100-pF source, 2 μV (-114 dBV) for a 1000-pF source, and 1.3 μV (-118 dBV) for a 1-μF source (input short circuited).

Theoretical considerations of the self-noise compare favorably with the actual values measured on the preamplifier. The hydrophone input circuit can be effectively modeled for a specific sensor-input stage as outlined in Ref. 1.

SUMMARY

This report has described in some detail the hydrophone preamplifier shown in Fig. 1, with dc and low-frequency ac analyses being given, including examples. Variations to the basic circuit were mentioned. Finally, an account was given of a hybrid IC implementation and its advantages.

REFERENCE

1. A. C. Tims, "Hydrophone Preamplifier Optimization—Prediction of Hydrophone Self Noise by a Noise Model," NRL Report 8180, Mar. 1978.

Appendix A

PARAMETER DEFINITIONS

f	frequency of sinusoidal input signal, in Hz
g_{m_1}	transconductance of Q_1, given by $g_{m_1} = i_c/v_{be}, v_{ce} = 0$
g_{m_2}	transconductance of Q_2, given by $g_{m_2} = i_d/v_{gs}, v_{ds} = 0$
h_{fe}	small-signal current gain of Q_1, given by $h_{fe} = i_c/i_b, v_{ce} = 0$
h_{oe}	output admittance of Q_1, given by $h_{oe} = i_c/v_{ce}, i_b = 0$
i	small-signal ac current
i_b	ac base current in Q_1
i_c	ac collector current in Q_1
i_d	ac drain current in Q_2
i_o	preamplifier ac output current
I_C	dc collector current in Q_1
I_D	dc drain current in Q_2
I_{DSS}	saturated dc drain current for Q_2 (with $V_{GS} = 0$)
I_E	dc emitter current in Q_1
r_d	reciprocal of h_{oe}
r_ℓ	parallel combination of R_L and r_d
r_π	small-signal input resistance of Q_1, given by $r_\pi = v_{be}/i_b, V_{ce} = 0$
R_{EQ}	parallel combination of R_1 and R_7, plus R_4 (Fig. 5)
R_L	preamplifier load resistance
R_P	parallel combination of R_2 and r_π
T_A	ambient temperature
v_1	equivalent to v_{be}
v_2	equivalent to v_{gs}
v_{be}	ac small-signal base-to-emitter voltage on Q_1
v_c	ac small-signal collector voltage on Q_1
v_{ce}	ac small-signal collector-to-emitter voltage on Q_1
v_{ds}	ac small-signal drain-to-source voltage on Q_2
v_{gs}	ac small-signal gate-to-source voltage on Q_2

v_i	ac input signal developed by the transducer
v_o	preamplifier ac output voltage
$+v_o$ MAX	peak positive value of v_o before clipping or distortion
$-v_o$ MAX	peak negative value of v_o before clipping or distortion
v_s	ac small-signal source voltage on Q_2
V_C	dc collector voltage on Q_1
V_{CC}	dc supply voltage to the preamplifier
V_{CE}	dc collector-to-emitter voltage on Q_1
V_D	dc drain voltage on Q_2
V_{DS}	dc drain-to-source voltage on Q_2
V_E	dc emitter voltage on Q_1
V_{EB}	dc emitter-to-base voltage on Q_1
V_G	dc gate voltage on Q_2
V_{GS}	dc gate-to-source voltage on Q_2
V_P	gate-to-source pinchoff voltage for Q_2
V_S	dc source voltage on Q_2
Z_o	ac small-signal low-frequency preamplifier output impedance

Appendix B
IMPORTANT EQUATIONS

For proper JFET biasing

$$I_D < I_{DSS}, \tag{1}$$

$$V_{DS} \geqslant V_{GS} - V_P, \tag{2}$$

and

$$0 > V_{GS} > V_P. \tag{25}$$

The drain current in a properly biased JFET is

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2. \tag{3}$$

The preamplifier gain is

$$G = \frac{v_o}{v_i} = \frac{g_{m_2} r_\ell (A + g_{m_1} R_P R_5)}{(R_5 + r_\ell)(A\, g_{m_2} + 1)}, \tag{39}$$

where

$$A = \frac{R_6[R_5 + r_\ell(1 + g_{m_1} R_P)]}{R_5 + r_\ell + R_6}. \tag{32}$$

The preamplifier output impedance is

$$Z_o = \frac{r_d[R_5 + R_6(1 + g_{m_2} R_5)]}{R_5 + R_6(1 + g_{m_2} R_5) + r_d[1 + g_{m_2} R_6(1 + g_{m_1} R_P)]}. \tag{55}$$

The preamplifier peak output ($R_L = \infty$) in the positive direction is

$$+ v_o \text{ MAX} \approx V_E - V_C \tag{45}$$

and in the negative direction is

$$- v_o \text{ MAX} \approx (V_C - V_S)\left(\frac{R_5 + R_6}{R_5}\right). \tag{47}$$

Appendix C
SELECTION OF DISCRETE COMPONENTS

The hybrid circuit described in this report has for some time been used in its discrete component form. For some low-noise hydrophone designs, use of the discrete form will probably continue.

The choice of components is important if an optimum circuit is to be realized. Low-noise metal-film resistors and low-noise transistors should be used. Reliable military-specified components are highly recommended, especially for deep-submergence long-life hydrophone applications. Voltage and power capabilities of all components must exceed the worst-case values possible in a given circuit.

At USRD, type CSR 13 solid tantalum, established-reliability, MIL-C-39003 capacitors are used for C_2 and C_3, and C_1 is a CK05 ceramic capacitor, MIL-C-11015. Established-reliability type CKR06 ceramic capacitors, MIL-C-39014, may be used for C_1. Resistors R_1, R_2, R_3, R_5, R_6, and R_7 are 1%-tolerance type RN55C metal-film resistors, MIL-R-10509. Resistor R_4 is a high-megohm resistive-glass component meeting MIL-STD-55182.

Special consideration should be given to the selection of high-megohm resistors. These can be obtained from several sources, and some are not adequately covered by a military specification. More importantly the high-megohm types can have a high-noise index and thus significantly degrade the self-noise performance of the preamplifier. A specific manufacturer or type should be selected only after a noise evaluation of the resistors has been made.

Special attention also needs to be given to the choice of Q_2. Most USRD designs use the 2N4867A JFET, an ultralow-noise device meeting MIL-S-19500. However some low-noise designs might use the 2N6451-2N6454 series of JFETS. If there are no restrictions on the power required for a hydrophone, the 2N6550 JFET may be considered.

Transistor Q_1 is not as critical as Q_2 from a noise standpoint. The 2N3251A PNP device works nicely in most designs.

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